**STIMULATION AND CHARACTERIZATION OF NANO SCALED FET**

**Submitted**

**By**

**Niharika Sidda [BU21EECE0100374]**

**Pasupuleti Sushanth[BU21EECE0100466]**

**Jillela Mounika[BU21EECE0100448]**

**Under the Guidance of [16 Bold]**

**(Dr.Ajit Kumar)**

**(Duration: 22/07/2024 to 23/10/2024)**



**Department of Electrical,Electronics and Communication Engineering [14 Bold]**

**GITAM School of Technology**

**GITAM**

**(DEEMED TO BE UNIVERSITY)**

**(Estd. u/s 3 of the UGC act 1956)**

**NH 207, Nagadenehalli, Doddaballapur taluk, Bengaluru-561203 Karnataka, INDIA.**

**DECLARATION**

**I/We declare that the project work contained in this report is original and it has been done by me under the guidance of my project guide.**

**Name: Niharika Sidda**

**Pasupuleti Sushanth**

**Jillela Mounika**

**Date: Signature of the Student**

**Department of Electrical,Electronics and Communication Engineering**

**GITAM School of Technology, Bengaluru-561203**

****

**CERTIFICATE**

**This is to certify that Niharika Sidda,Pasupuleti Sushanth,Jillela Mounika bearing BU21EECE0100374,BU21EECE0100466,BU21EECE0100448 has satisfactorily completed Mini Project Entitled in partial fulfillment of the requirements as prescribed by University for VIIIth semester, Bachelor of Technology in “Electrical, Electronics and Communication Engineering” and submitted this report during the academic year 2024-2025.**

**[Signature of the Guide] [Signature of HOD]**

**Table of contents**

[**Chapter 1: Introduction 1**](#_heading=h.gjdgxs)

[1.1 Overview of the problem statement 1](#_heading=h.30j0zll)

[1.2 Objectives and goals 1](#_heading=h.1fob9te)

[**Chapter 2 : Literature Review 2**](#_heading=h.3znysh7)

[**Chapter 3 : Strategic Analysis and Problem Definition 3**](#_heading=h.2et92p0)

[3.1 SWOT Analysis 3](#_heading=h.tyjcwt)

[3.2 Project Plan - GANTT Chart 3](#_heading=h.1t3h5sf)

[3.3 Refinement of problem statement 3](#_heading=h.2s8eyo1)

[**Chapter 4 : Methodology 4**](#_heading=h.17dp8vu)

[4.1 Description of the approach 4](#_heading=h.3rdcrjn)

[4.2 Tools and techniques utilized 4](#_heading=h.26in1rg)

[4.3 Design considerations 4](#_heading=h.lnxbz9)

[**Chapter 5 : Implementation 5**](#_heading=h.1ksv4uv)

[5.1 Description of how the project was executed 5](#_heading=h.44sinio)

[5.2 Challenges faced and solutions implemented 5](#_heading=h.2jxsxqh)

[**Chapter 6:Results 6**](#_heading=h.z337ya)

[6.1 outcomes 6](#_heading=h.3j2qqm3)

[6.2 Interpretation of results 6](#_heading=h.1y810tw)

[6.3 Comparison with existing literature or technologies 6](#_heading=h.2xcytpi)

[**Chapter 7: Conclusion 7**](#_heading=h.1ci93xb)

[**Chapter 8 : Future Work 8**](#_heading=h.2bn6wsx)

[Here write Suggestions for further research or development Potential improvements or extensions 8](#_heading=h.qsh70q)

[**References 9**](#_heading=h.1pxezwc)

# 

# 

# **Chapter 1: Introduction:**

Nanoscaled Field-Effect Transistors (FETs) are tiny electronic components used in modern devices like smartphones and computers. As technology advances, these FETs are becoming smaller and more complex, making their behavior harder to predict and understand. To address this,we use simulation and characterization techniques to make it easier.

**Simulation** is like creating a digital twin of the FET. By using computer models, we can predict how the FET will behave under different conditions. This helps in understanding the effects of tiny imperfections and variations that are inevitable at such small scales. Simulations allow us to test various designs and materials virtually, saving time and cost compared to building and testing real prototypes.

**Characterization** involves studying the actual physical FETs to measure their properties and performance. This is done using specialized tools that can detect very small changes in the FET's behavior. By combining simulation and characterization, we can ensure that the FETs will work reliably in real-world applications, even as they continue to shrink in size.

## **1.1 Overview of the problem statement:**

The problem involves simulating and characterizing a nanoscale FET to analyze its performance and address challenges like short-channel effects and quantum tunneling. The goal is to optimize the device design for better control over leakage and switching. Simulations will help refine the doping profile, structure, and material choices to improve transistor efficiency at the nanoscale.

## **1.2 Objectives and goals:**

The objective of stimulating and characterizing nanoscale FETs is to understand their behavior, optimize their performance, and ensure reliability at such small scales. It involves testing how they function under different conditions, identifying any limitations, and finding ways to improve their efficiency. The goal is to test how these tiny electronic switches perform and to measure their key properties, like speed and efficiency. This helps in improving their design and ensuring they work reliably.

**Main Goals**

* Performance Optimization
* Understanding Behavior
* Scaling Down Further
* Exploring New Materials

# **Chapter 2 : Literature Review:**

| **TITLE** | **AUTHOR** | **YEAR** | **TECHNOLOGY USED** | **SUMMARY** | **PRO** | **LIMITATION** |
| --- | --- | --- | --- | --- | --- | --- |
| Device and circuit performance analysis of double gate junctionless transistors at Lg = 18 nm | Chitrakant Sahu,  Jawar Singh | 2014 | ATLAS TCAD mixed-mode simulator | JL DG devices outperform IM FETs with better speed and stability. | Faster performance and improved SRAM stability | JL design complexity compared to conventional CMOS. |
| Analysis of Delta-Doped and Uniformly Doped AlGaAs/GaAs HEMTs by Ensemble Monte Carlo Simulations | Ki Wook Kim, Hong Tian, Michael A. Littlejohn | 1991 | Uniformly doped AlGaAs/GaAs high electron mobility transistors (HEMTs) | Delta-doped HEMTs outperform uniform ones in electron density and speed. | Improved transconductance and drain current drive | Increased complexity in device structure and fabrication. |

| **TITLE** | **AUTHOR** | **YEAR** | **TECHNOLOGY USED** | **SUMMARY** | **PRO** | **LIMITATION** |
| --- | --- | --- | --- | --- | --- | --- |
| A Physics-Based Threshold Voltage Model for Junctionless Double Gate FETs Having Vertical Structural and Doping Asymmetry | A. Kumar,  J. N. Roy | 2019 | Synopsys Sentaurus Device simulation tool,  MATLAB | Model for asymmetric JL DG FETs simplifies analysis while maintaining accuracy | Simplifies complex calculations with improved accuracy. | May not account for all real-world device variations. |
| Impact of Single Charged Gate Oxide Defects on the Performance and Scaling of Nanoscaled FETs | J. Franco, B. Kaczer, M. Toledano-Luque, et al. | 2012 | Nanoscaled Field-Effect Transistors (FETs)  particularly pFinFETs and planar pMOSFETs, which include SiGe channel devices | NBTI reliability in nanoscaled FETs varies by technology, impacting scaling | SiGe channel devices exhibit reduced time-dependent variability, enhancing NBTI robustness. | The severe 1/area scaling rule complicates reliability predictions for further scaling. |

| **TITLE** | **AUTHOR** | **YEAR** | **TECHNOLOGY USED** | **SUMMARY** | **PRO** | **LIMITATION** |
| --- | --- | --- | --- | --- | --- | --- |
| Thermo-magnetic effects on MOSFETs simulated and experimentally characterized for reliability 5th | Gabriela A. Rodríguez-Ruiz et al. | 2015 | Thermo-magnetic modeling and simulation in nano-scaled MOSFETs. | The paper introduces a simulation method for studying the effects of temperature and magnetic fields on the gate tunneling current in MOSFET devices. | Provides a new method for mapping electronic properties in nanoscaled MOSFETs. | Simulation and experimental setup are complex and require precise control. |

# **Chapter 3 : Strategic Analysis and Problem Definition:**

# **3.1 SWOT Analysis:**

SWOT Analysis is defined as Strengths,Weaknesses,Opportunities & Threats. Here’s the SWOT Analysis:

### 

### **Strengths:** **Weaknesses:**

1.Precise Analysis 1.Simulation Accuracy

2.Time-Saving 2.Assumptions Approximations

3.Enhanced Optimization

**Opportunities: Threats:**

1.Technology Advancement 1.Rapid Technological Changes

2.Integration with AI/ML 2.High Competition

3.Miniaturization Trend 3.Data Security Risks

4.Cross-Disciplinary Collaboration

# **Chapter 4 : Methodology:**

* **Device Modeling**: Computational models, such as **TCAD (Technology Computer-Aided Design)**, are used to simulate the electrical behavior of nano-FETs. The models incorporate quantum mechanical effects, which are critical at the nanoscale.
* **Electrical Characterization**: Once the FET is fabricated, key electrical parameters such as **current-voltage (I-V) characteristics**, **threshold voltage (Vth)**, **subthreshold slope**, and **on-off current ratio** are measured.

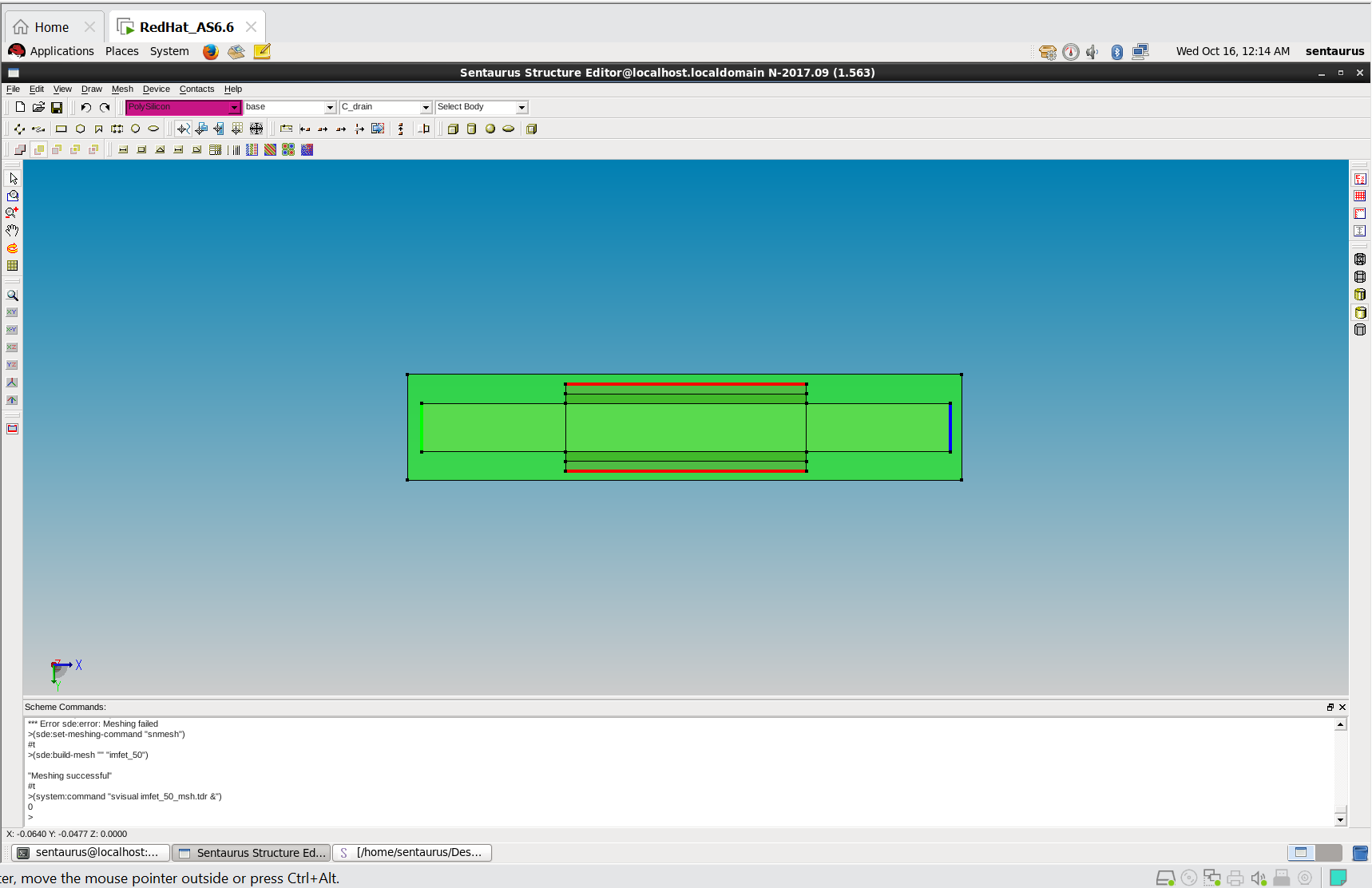
### **4.1 Tools and techniques utilized:**

* **Design Specifications:** Define key parameters such as channel length, width, and material properties.Use CAD tools like TCAD.
* **Material Selection:** Choose suitable semiconductor materials (e.g., silicon, graphene, MoS2) based on desired electrical properties and scalability.
* **Current-Voltage (I-V) Testing**: Measures how much current flows through the FET at different voltages. This shows how well the FET turns on and off.
* **Capacitance-Voltage (C-V) Measurements**: Checks how the gate (control part) of the FET responds to changes in voltage, which affects speed and power consumption.

#### **4.3 Design considerations:**

* **Scaling and Size**: As transistors get smaller, controlling short-channel effects (SCE) like leakage current and Drain-Induced Barrier Lowering (DIBL) becomes more difficult. Proper scaling is essential to maintain efficiency.
* **Material Selection**: Using advanced materials, such as high-k dielectrics (for gate insulation) or new semiconductors like GaN or graphene, can enhance performance by reducing leakage and improving speed.
* **Quantum Effects**: At the nanoscale, quantum mechanical effects like tunneling and electron confinement significantly impact device behavior, so they need to be considered in design.
* **Power Consumption**: Reducing power consumption is critical, especially for low-power applications. Techniques like using multi-gate architectures (FinFETs) help reduce power while maintaining high performance.

**Chapter 5 : Implementation:**

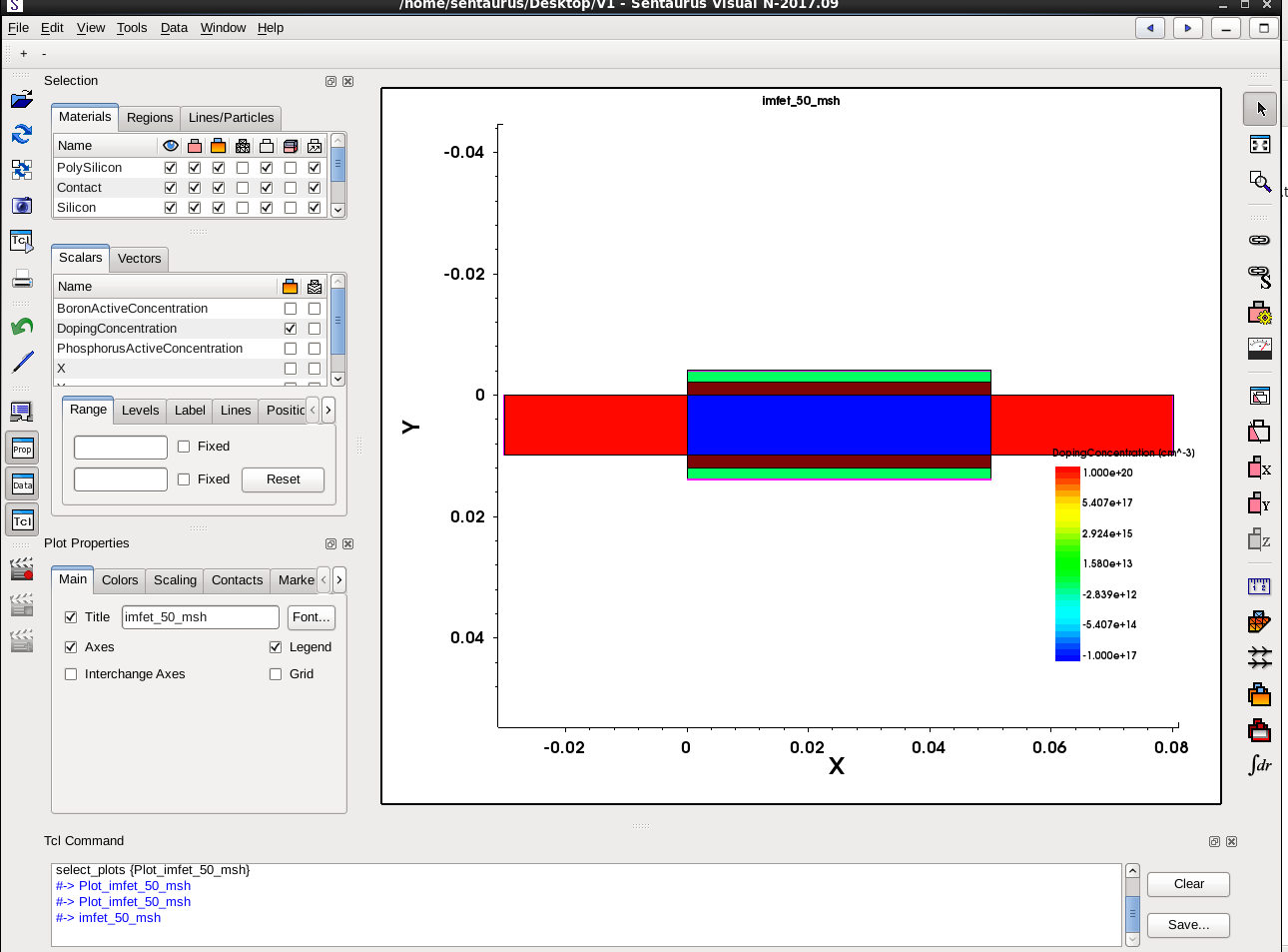


## 

## **5.1 Description of how the project was executed**

The green area represents the semiconductor material (likely silicon), while the black lines outline the key boundaries of the transistor. The red lines likely indicate contact regions for the source and drain. This structure defines the physical dimensions and layout of the transistor, which will be used in further simulations to analyze its electrical properties.

# **Chapter 6:Results**



## 

# **Chapter 7: Conclusion:**

* **Simulation Overview**: This tells about the structure of the nanoscale transistor with different regions like silicon, polysilicon, and contacts. The color-coded doping concentrations indicate that the source, drain, and channel regions are clearly defined, which is necessary for the transistor to work.
* **Output Characteristics**: It shows how the drain current (output) increases as we apply more voltage to the gate (input).
* Some advanced effects that happen when transistors get very small (like short-channel and quantum effects) need further study to improve accuracy.

# **Chapter 8 : Challenges & Future Work:**

**Challenges :**

**Short-Channel Effects:** As FETs get smaller, the control of the gate over the channel (where current flows) becomes weaker, which again leads to poor performance and higher power consumption.

**Heat and Reliability**: Smaller devices generate more heat, which affects reliability and lifespan.

**Future Work** :

**Advanced Measurement Techniques**: As the devices shrinks in size the general methods may not be precise enough to work with so we will need new techniques to measure its properties accordingly.

**Reliability Testing**: As we already talked since the size shrinks testing reliability under various conditions like heat,voltage,temperature becomes more crucial, more advanced techniques will be introduced to make sure that nano scaled FETs are strong.

# **References:**

**Chitrakant Sahu, Jawar Singh.** "Device and circuit performance analysis of double gate junctionless transistors at Lg = 18 nm." *The Journal of Engineering*, 2014, Vol. 2014, Iss. 3, pp. 105–110. DOI: 10.1049/joe.2013.0269

**.** Kim, K. W., Tian, H., & Littlejohn, M. A. (1991). "Analysis of delta-doped and uniformly doped AlGaAs/GaAs HEMT's by ensemble Monte Carlo simulations," *IEEE Transactions on Electron Devices*, 38(8), 1731-1741

**.** H. Horie et al., 1991,C.-W. Lee et al., 2009&R. Rios et al., 2011 0018-9383 © 2019 IEEE

**.** J. Franco et al., "Superior NBTI Reliability of SiGe Channel pMOSFETs," Proc. IEDM, 2011

T. Grasser et al., "Recent Advances in Understanding the Bias Temperature Instability," Proc. IEEE IEDM, 2010

**.** Rodríguez-Ruiz, G. A., Gutiérrez-D, E. A., Sarmiento-Reyes, L. A., Stanojevic, Z., Kosina, H., Guarin, F. J., & García-R, P. J. (2015). *Thermo-Magnetic Effects in Nano-Scaled MOSFET: An Experimental, Modeling, and Simulation Approach.* IEEE Journal of the Electron Devices Society, 3(2), 78-84. DOI: 10.1109/JEDS.2015.2390629.

**Github Link:**